Notice of Allowability	Application No.	Applicant(s)	
	10/722,559	TERUI, MAKOTO	
	Examiner	Art Unit	
	Tuan Quach	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to _____.

2. ☒ The allowed claim(s) is/are *1-14*.

3. ☒ The drawings filed on *22 April 2004* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below.. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 4/22/04
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Tuan Quach

Tuan Quach
Primary Examiner

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

Claims 1-14 are allowed primarily because the prior art of record singly or in combination do not teach or suggest combination to arrive at the claimed invention, including the claimed invention in claim 1 regarding a semiconductor device comprising a semiconductor substrate having a first region formed with a circuit element and provided with a plurality of circuit element connecting pads to which said circuit element is connected, and a second region surrounding said first region; the periphery of a first external terminal having a plurality of first sub-external terminals disposed on said first region and composed of terminals to be grounded and terminals to be connected to a power source, and a plurality of second sub-external terminals disposed on said first region; plurality of second external terminals disposed on said second region; a first wiring structure having a first sub-wiring structure provided on said first region for electrically connecting said plurality of first sub-external terminals and said plurality of circuit element connecting pads, and a second sub-wiring structure provided on said first region for electrically connecting said plurality of second sub-external terminals and said plurality of circuit element connecting pads; and a plurality of second wiring structures provided from said first region to said second region for electrically connecting said plurality of second external terminals and said plurality of circuit element connecting pads.

The prior art of record singly or in combination further do not teach

or suggest combination to arrive at the claimed invention, including the claimed invention in claim 5 regarding a semiconductor device comprising a semiconductor substrate having a first region with a plurality formed with a circuit element and provided circuit element connecting pads to which said circuit element is connected, and a second region surrounding the periphery said first region; metallic layer provided on said second region; an insulating film provided such that a part of said circuit element connecting pads and a part of said metallic layer are exposed; a plurality of first wiring structures provided on said insulating film in said first region and electrically connected to said plurality of circuit element connecting pads; a plurality of second wiring structures provided on said insulating film from said first region to said second region and electrically connected to said plurality of circuit element connecting pads; a plurality of third wiring structures provided on said insulating film in said second region and connected to said exposed metallic layer; electrically a sealing portion provided such that a part of said first wiring structures is exposed and such that a part of said second wiring structures and third wiring structures is exposed in said second region; a plurality of first external terminals disposed on said first region and connected to said first wiring structures; and a plurality of second external terminals disposed on said second region and connected to one or both of said second wiring structures and said third wiring structures.

The prior art of record singly or in combination also do not teach or suggest combination to arrive at the claimed invention, including the claimed invention in claim 10 regarding a semiconductor device comprising a semiconductor substrate having a

first region formed with a circuit element and provided with a plurality of circuit element connecting pads to which said circuit element is connected, and a second region surrounding the periphery of said first region; a metallic layer provided on said second region; an insulating film provided such that a part of said circuit element connecting pads and a part of said metallic layer are exposed; a first wiring structure having a first sub-wiring structure provided on said insulating film in said first region and electrically connected to said plurality of circuit element connecting pads, and a second sub-wiring structure provided on said insulating film in said first region and electrically connected to said plurality of circuit element connecting pads; a plurality of second wiring structures provided on said insulating film from said first region to said second region and electrically connected to said circuit element connecting pads; a plurality of third wiring structures provided on said insulating in said second region and electrically connected to said exposed metallic layer; a sealing portion provided such that a part of said first sub-wiring structure and said second sub-wiring structure is exposed, and such that a part of said second wiring structure and said third wiring structure in said second region is exposed; a first external terminal having a plurality of first sub-external terminals disposed on said first region and composed of terminals to be connected to a power source, and a plurality of second sub-external terminals disposed on said first region; and a plurality of second external terminals disposed on said second region and connected to one or both of said second wiring structure and said third wiring structure.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Quach whose telephone number (571) 272-1717. The examiner can normally be reached on M - F from 8 to 4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-1562.

TQuach

Tuan Quach
Primary Examiner